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(54) **SYSTEMS AND METHODS FOR RECOVERED DATA STITCHING**

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(51) **Int. Cl.**

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H03M 13/00	(2006.01)
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G06F 11/10	(2006.01)
G11B 20/10	(2006.01)
G11B 20/18	(2006.01)

(52) **U.S. Cl.**

CPC ***G06F 17/30135*** (2013.01); ***G06F 11/085*** (2013.01); ***G06F 11/1076*** (2013.01); ***G11B 20/10009*** (2013.01); ***G11B 20/10268*** (2013.01); ***G11B 20/18*** (2013.01); ***G11B 20/1866*** (2013.01)

(58) **Field of Classification Search**

None

See application file for complete search history.

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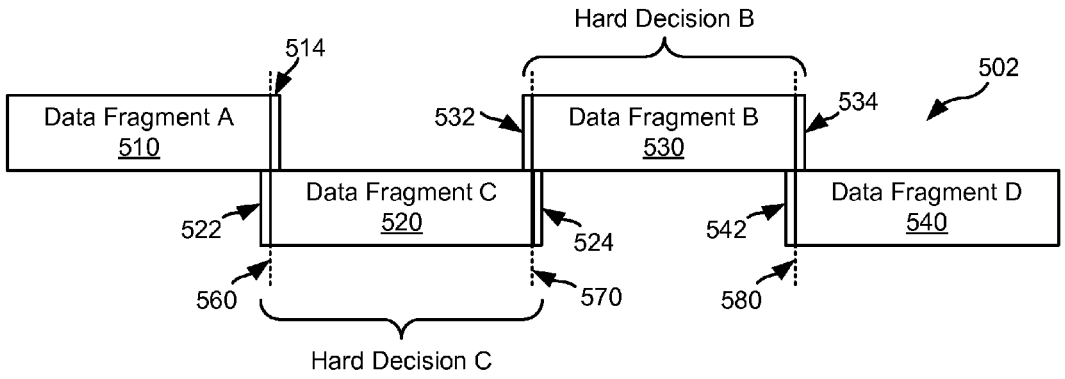
Primary Examiner — Daniel McMahon

(57) **ABSTRACT**

Systems and method relating generally to data processing, and more particularly to systems and methods for combining recovered portions of a data set. In one particular case, a system is disclosed that includes a stitching circuit and a data recovery circuit. The stitching circuit is operable to: receive a data set including at least a first fragment and a second fragment; replicate data from at least one of the first fragment and the second fragment as stitching values; and aggregate the first fragment with the second fragment with the stitching values between the first fragment and the second fragment to yield a combined data set. The data recovery circuit is operable to process the combined data set to yield an original data set.

20 Claims, 7 Drawing Sheets



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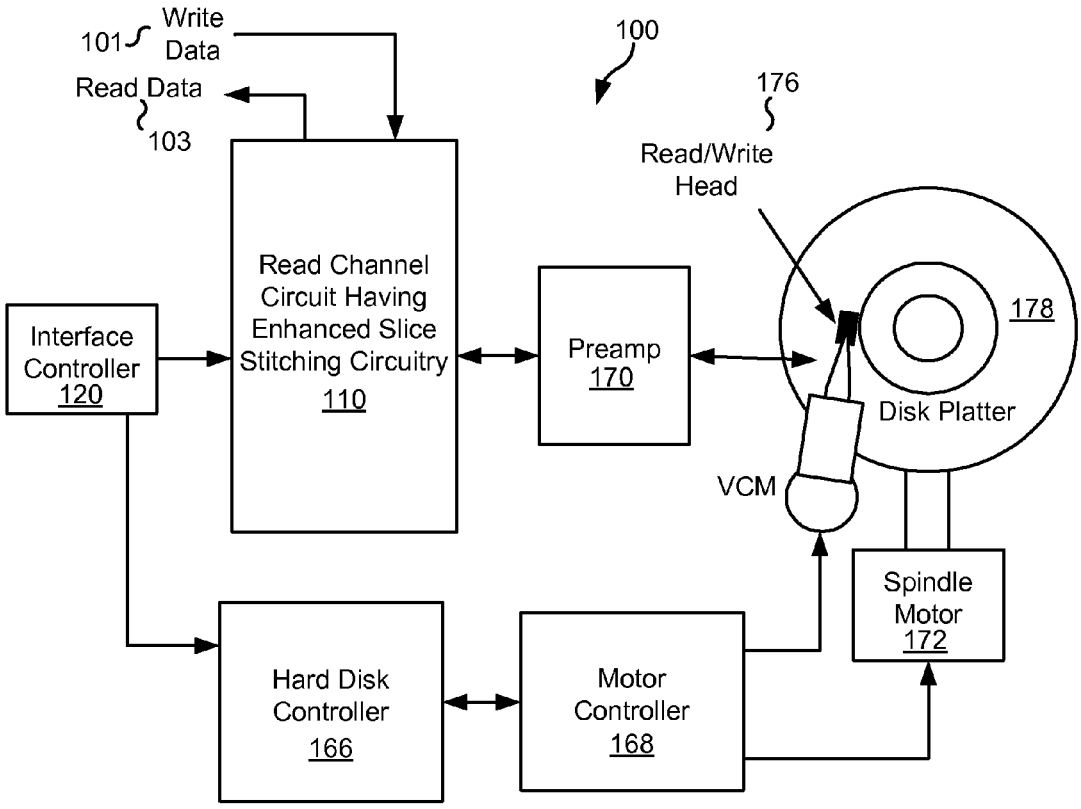
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Read Data
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Preamp
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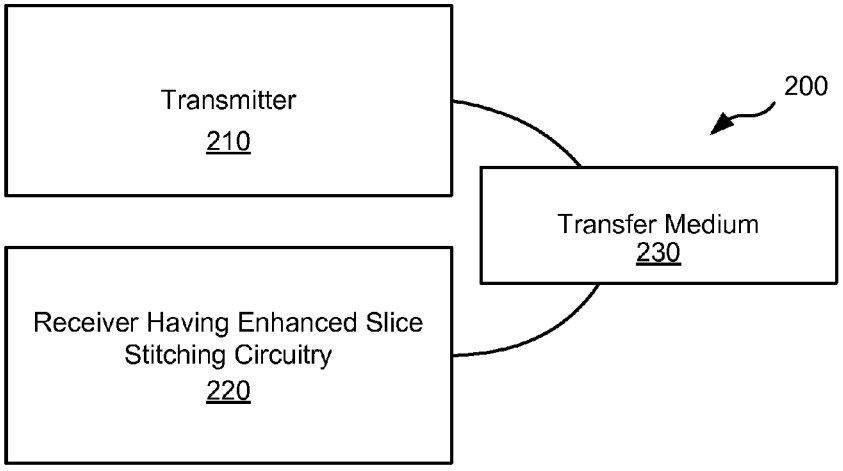
Disk Platter
VCM
Spindle Motor
172
Hard Disk Controller
166
Motor Controller
168

Fig. 1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Transfer Medium
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Receiver Having Enhanced Slice Stitching Circuitry
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Fig. 2

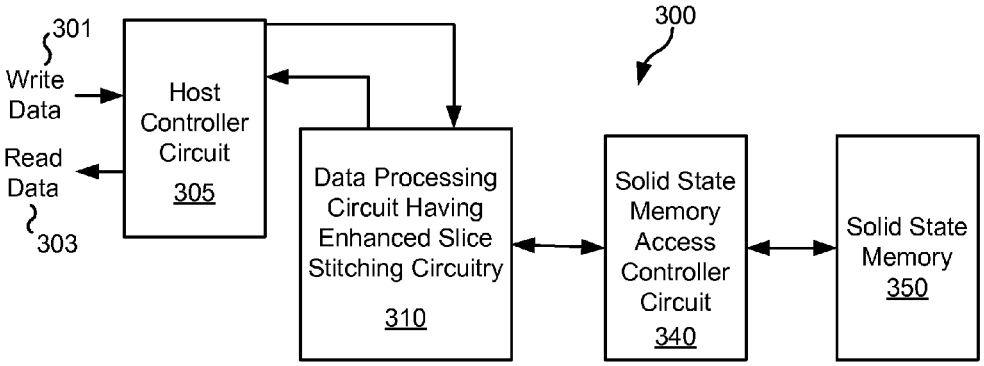
301
Write Data
Read Data
303
Host Controller Circuit
305
300
Data Processing Circuit Having Enhanced Slice Stitching Circuitry
310
Solid State Memory Access Controller Circuit
340
Solid State Memory
350

Fig. 3

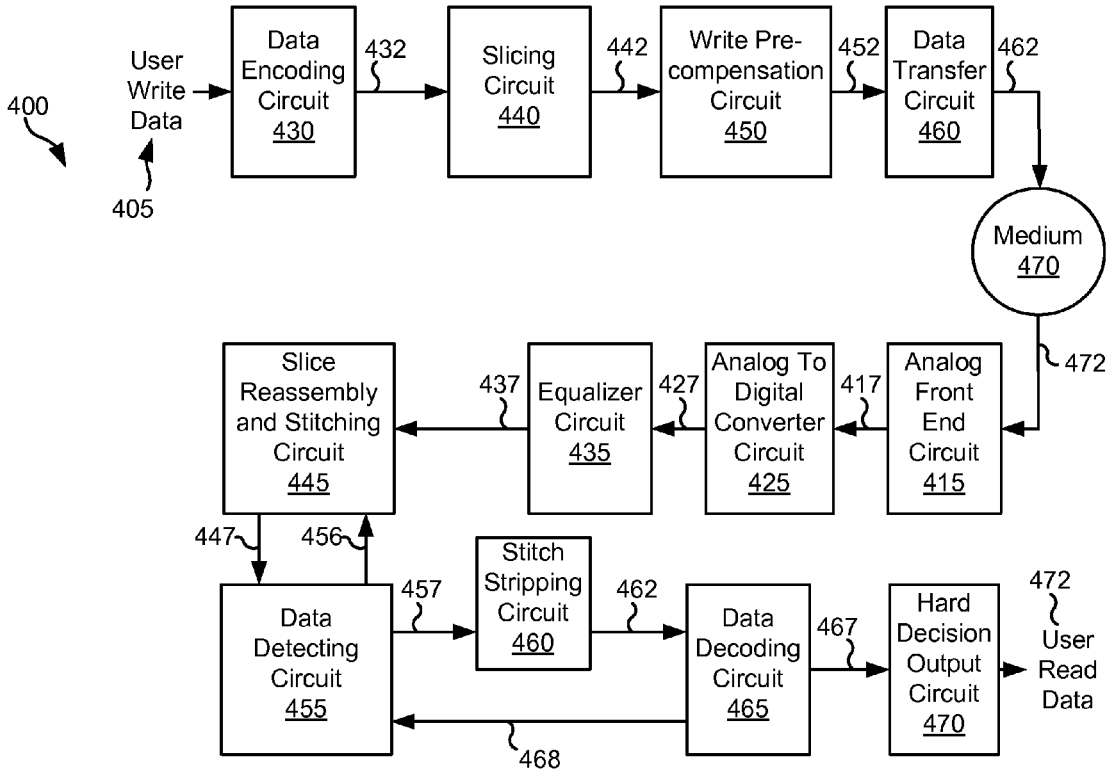
400
User Write Data
405
Data Encoding Circuit
430
432
Slicing Circuit
440
442
Write Pre-compensation Circuit
450
452
Data Transfer Circuit
460
462
Medium
470
472
Analog Front End Circuit
415
417
Analog To Digital Converter Circuit
425
427
Equalizer Circuit
435
437
Slice Reassembly and Stitching Circuit
445
447
456
Data Detecting Circuit
455
457
Stitch Stripping Circuit
460
462
Data Decoding Circuit
465
467
Hard Decision Output Circuit
470
472
User Read Data
468

Fig. 4

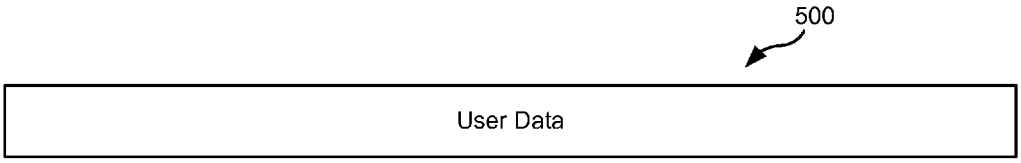

Fig. 5a

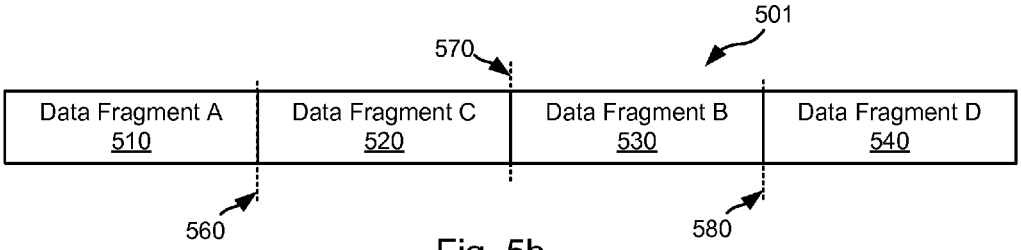

Fig. 5b

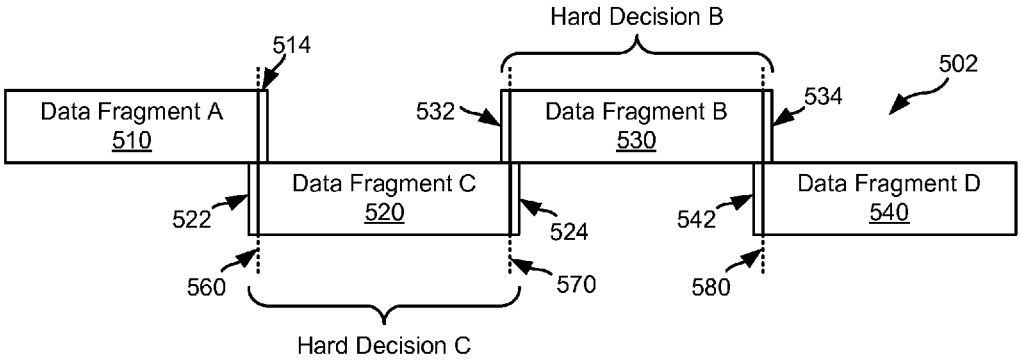

Fig. 5C

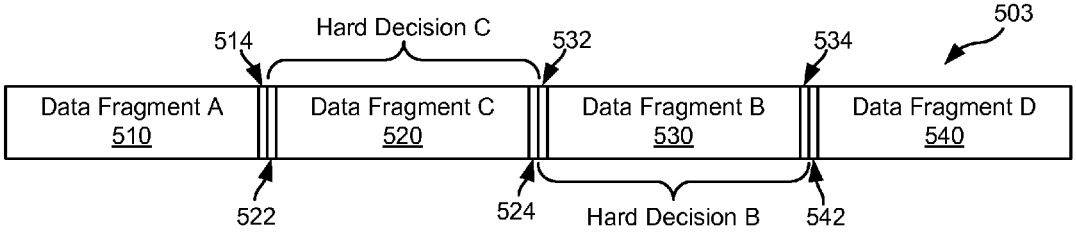

Fig. 5d

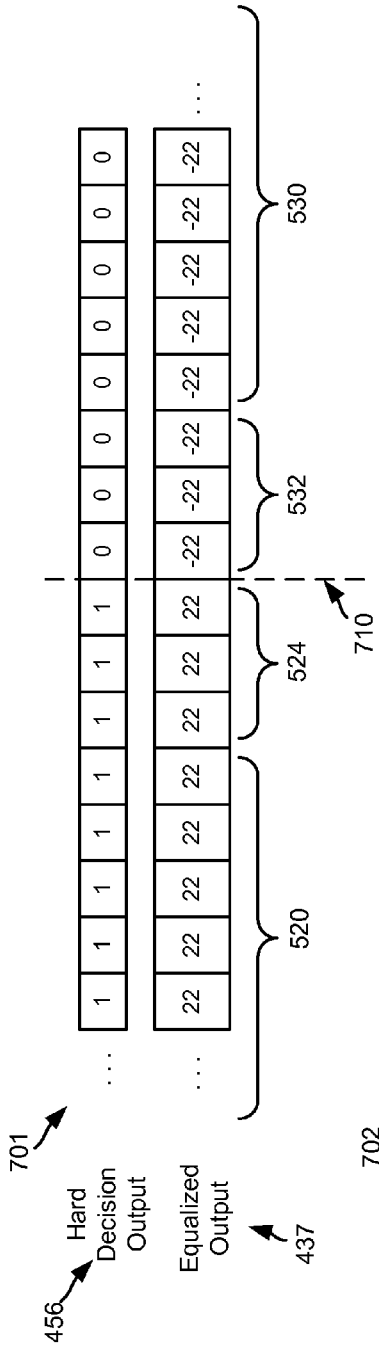

Fig. 7a

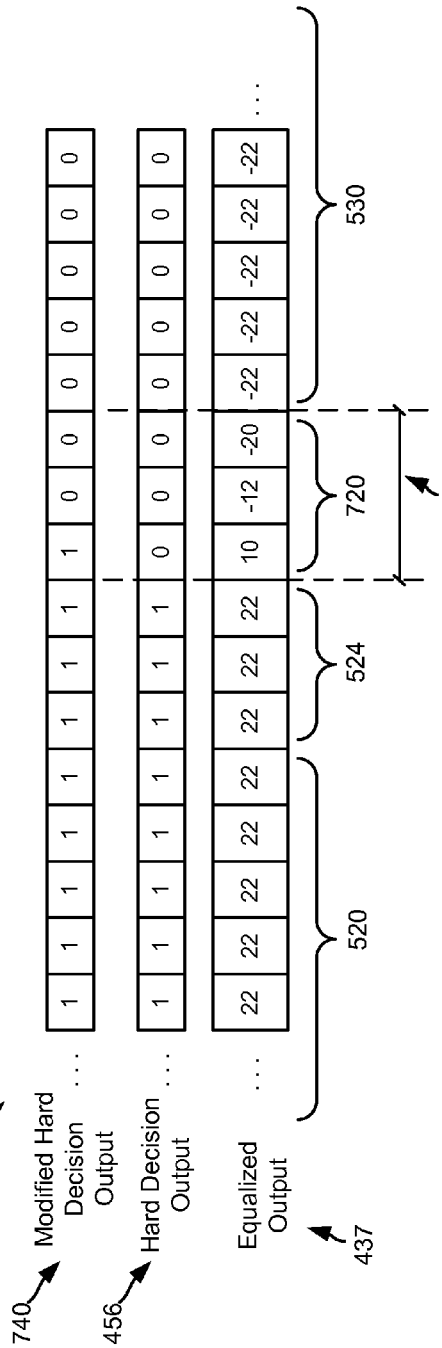

Fig. 7b

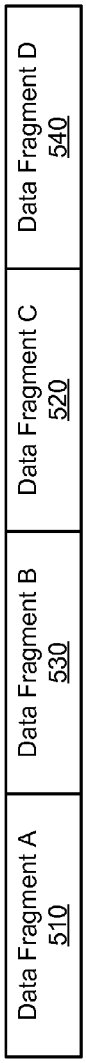

Fig. 5e

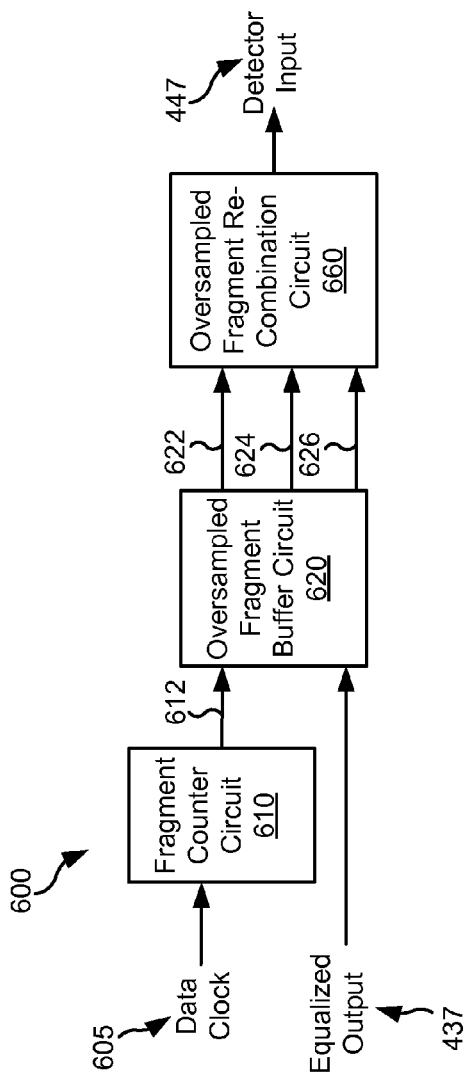
600
Fragment Counter Circuit 610
612
Oversampled Fragment Buffer Circuit 620
622
624
626
Oversampled Fragment Re-Combination Circuit 660
447
Detector Input
605
Data Clock
Equalized Output
437

Fig. 6

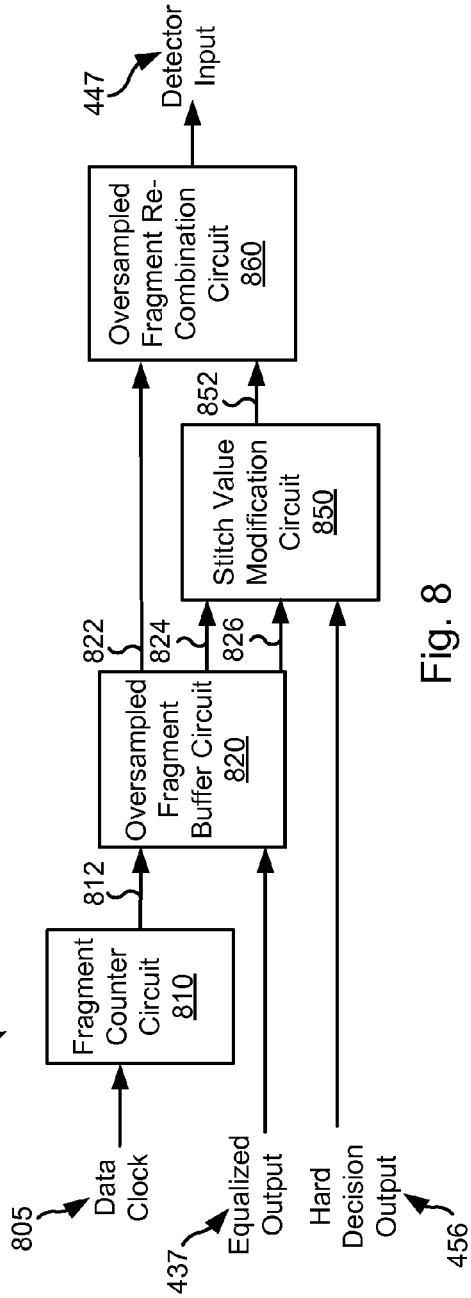
800
Fragment Counter Circuit 810
812
Oversampled Fragment Buffer Circuit 820
822
824
826
Stitch Value Modification Circuit 850
852
Oversampled Fragment Re-Combination Circuit 860
447
Detector Input
805
Data Clock
437
Equalized Output
Hard Decision Output
456

Fig. 8

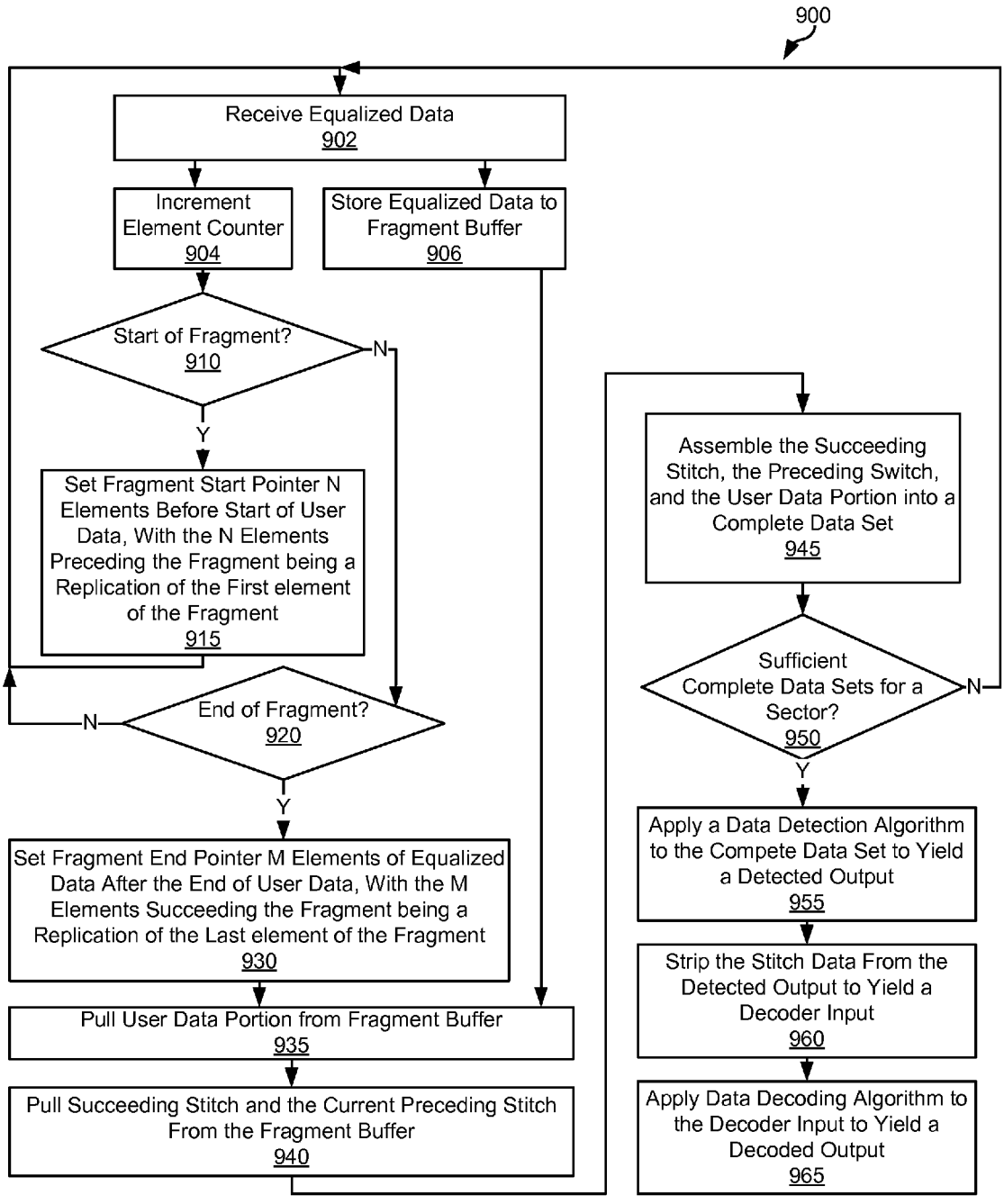
900
Receive Equalized Data
902
Increment Element Counter
904
Store Equalized Data to Fragment Buffer
906
Start of Fragment?
910
N
Y
Set Fragment Start Pointer N Elements Before Start of User Data, With the N Elements Preceding the Fragment being a Replication of the First element of the Fragment
915
End of Fragment?
920
N
Y
Set Fragment End Pointer M Elements of Equalized Data After the End of User Data, With the M Elements Succeeding the Fragment being a Replication of the Last element of the Fragment
930
Pull User Data Portion from Fragment Buffer
935
Pull Succeeding Stitch and the Current Preceding Stitch From the Fragment Buffer
940
Assemble the Succeeding Stitch, the Preceding Switch, and the User Data Portion into a Complete Data Set
945
Sufficient Complete Data Sets for a Sector?
950
N
Y
Apply a Data Detection Algorithm to the Compete Data Set to Yield a Detected Output
955
Strip the Stitch Data From the Detected Output to Yield a Decoder Input
960
Apply Data Decoding Algorithm to the Decoder Input to Yield a Decoded Output
965

Fig. 9

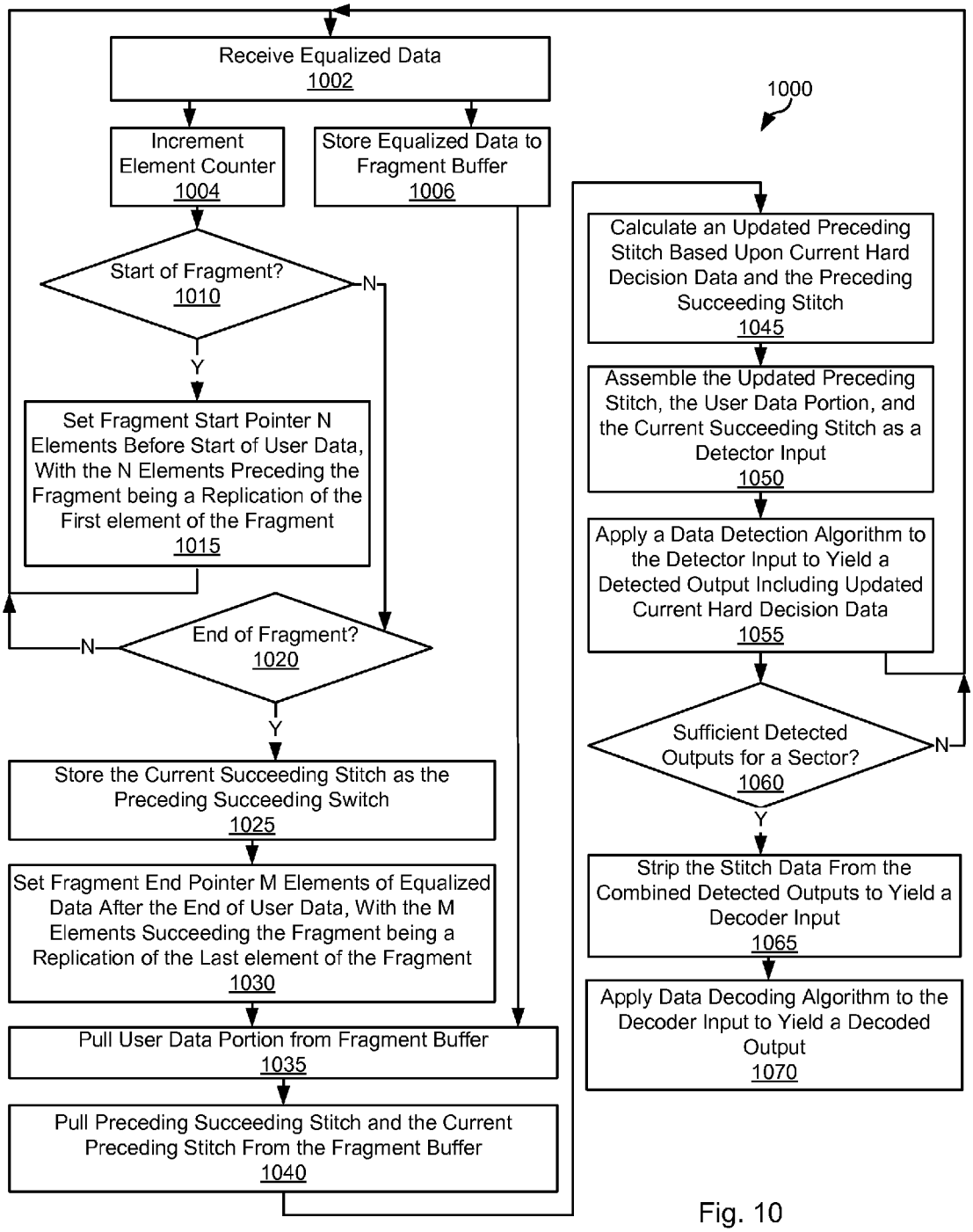
Receive Equalized Data
1002
1000
Increment Element Counter
1004
Store Equalized Data to Fragment Buffer
1006
Start of Fragment?
1010
N
Y
Set Fragment Start Pointer N Elements Before Start of User Data, With the N Elements Preceding the Fragment being a Replication of the First element of the Fragment
1015
End of Fragment?
1020
N
Y
Store the Current Succeeding Stitch as the Preceding Succeeding Switch
1025
Set Fragment End Pointer M Elements of Equalized Data After the End of User Data, With the M Elements Succeeding the Fragment being a Replication of the Last element of the Fragment
1030
Pull User Data Portion from Fragment Buffer
1035
Pull Preceding Succeeding Stitch and the Current Preceding Stitch From the Fragment Buffer
1040
Calculate an Updated Preceding Stitch Based Upon Current Hard Decision Data and the Preceding Succeeding Stitch
1045
Assemble the Updated Preceding Stitch, the User Data Portion, and the Current Succeeding Stitch as a Detector Input
1050
Apply a Data Detection Algorithm to the Detector Input to Yield a Detected Output Including Updated Current Hard Decision Data
1055
Sufficient Detected Outputs for a Sector?
1060
N
Y
Strip the Stitch Data From the Combined Detected Outputs to Yield a Decoder Input
1065
Apply Data Decoding Algorithm to the Decoder Input to Yield a Decoded Output
1070

Fig. 10

SYSTEMS AND METHODS FOR RECOVERED DATA STITCHING

CROSS REFERENCE TO RELATED APPLICATIONS

The present application claims priority to (is a non-provisional of) U.S. Pat. App. No. 61/878,678 entitled "Systems and Methods for Recovered Data Stitching", and filed Sep. 17, 2013 by Yang et al., and from U.S. Pat. App. No. 61/885,314 entitled "Systems and Methods for Fragmented Data Recovery", and filed Oct. 1, 2013 by Xia et al. The entirety of the aforementioned provisional patent applications is incorporated herein by reference for all purposes.

FIELD OF THE INVENTION

Systems and method relating generally to data processing, and more particularly to systems and methods for combining recovered portions of a data set.

BACKGROUND

Data transfer devices often packetize data prior to sending the data across a transfer medium. This transfer medium may be, for example, a data transmission medium or a storage medium. Once the packetized data is received, it is reassembled to yield the original data. In some cases, errors are introduced through the reassembly process.

Hence, for at least the aforementioned reasons, there exists a need in the art for advanced systems and methods for data processing.

SUMMARY

Systems and method relating generally to data processing, and more particularly to systems and methods for combining recovered portions of a data set.

Various embodiments of the present invention provide data processing systems that include a stitching circuit and a data recovery circuit. The stitching circuit is operable to: receive a data set including at least a first fragment and a second fragment; replicate data from at least one of the first fragment and the second fragment as stitching values; aggregate the first fragment with the second fragment with the stitching values between the first fragment and the second fragment to yield a combined data set; and a data recovery circuit operable to process the combined data set to yield an original data set.

This summary provides only a general outline of some embodiments of the invention. The phrases "in one embodiment," "according to one embodiment," "in various embodiments", "in one or more embodiments", "in particular embodiments" and the like generally mean the particular feature, structure, or characteristic following the phrase is included in at least one embodiment of the present invention, and may be included in more than one embodiment of the present invention. Importantly, such phases do not necessarily refer to the same embodiment. Many other embodiments of the invention will become more fully apparent from the following detailed description, the appended claims and the accompanying drawings.

BRIEF DESCRIPTION OF THE FIGURES

A further understanding of the various embodiments of the present invention may be realized by reference to the figures which are described in remaining portions of the specification. In the figures, like reference numerals are used throughout several figures to refer to similar components. In some instances, a sub-label consisting of a lower case letter is associated with a reference numeral to denote one of multiple similar components. When reference is made to a reference numeral without specification to an existing sub-label, it is intended to refer to all such multiple similar components.

FIG. **1** shows a storage device including a read channel circuit having enhanced slice stitching circuitry in accordance with various embodiments of the present invention;

FIG. **2** shows a data transmission device including a receiver having enhanced slice stitching circuitry in accordance with one or more embodiments of the present invention;

FIG. **3** shows a solid state memory circuit including a data processing circuit having enhanced slice stitching circuitry in accordance with some embodiments of the present invention;

FIG. **4** shows a data transfer circuit transferring data via a medium and including a slice reassembly and stitching circuit in accordance with various embodiments of the present invention;

FIGS. **5***a*-**5***e* graphically depict data processing in accordance with some embodiments of the present invention;

FIG. **6** shows a detailed block diagram of a data reassembly and stitching circuit in accordance with one or more embodiments of the present invention;

FIG. **7***a* graphically depicts data stitching without stitch value modification in accordance with some embodiments of the present invention;

FIG. **7***b* graphically depicts data stitching including stitch value modification in accordance with other embodiments of the present invention;

FIG. **8** shows a detailed block diagram of a data reassembly and stitching circuit including a stitch value modification circuit in accordance with some embodiments of the present invention;

FIG. **9** is a flow diagram showing a method in accordance with some embodiments of the present invention for data reassembly and stitching without stitch value modification; and

FIG. **10** is a flow diagram showing a method in accordance with other embodiments of the present invention for data reassembly and stitching including stitch value modification.

DETAILED DESCRIPTION OF SOME EMBODIMENTS

Systems and method relating generally to data processing, and more particularly to systems and methods for combining recovered portions of a data set.

Various embodiments of the present invention provide data processing systems that include a stitching circuit and a data recovery circuit. The stitching circuit is operable to: receive a data set including at least a first fragment and a second fragment; replicate data from at least one of the first fragment and the second fragment as stitching values; aggregate the first fragment with the second fragment with the stitching values between the first fragment and the second fragment to yield a combined data set; and a data recovery circuit operable to process the combined data set to yield an original data set. In some cases, the system is implemented as part of a communication device. In other instances, the system is implemented as part of a storage device. In particular cases, the system is implemented as part of an integrated circuit.

In some instances of the aforementioned embodiments, the stitching circuit includes a stitch value modification circuit that is operable to modify at least one of the stitching values

to a transitional value between the last element of the first fragment and the first element of the second fragment. In such instances, aggregating the first fragment with the second fragment includes the modified stitching values between the first fragment and the second fragment. In some such instances, the data recovery circuit generates at least one hard decision output corresponding to the combined data set, and the transitional value is generated by the stitch value modification circuit based at least in part on the hard decision output. In one or more of the aforementioned embodiments, the transitional value smoothes a discontinuity between the first fragment and the second fragment.

In various instances of the aforementioned embodiments, replicating data from at least one of the first fragment and the second fragment as stitching values includes: replicating a value from the first fragment as a first set of stitching values, and replicating a value from the second fragment as a second set of stitching values. In such instances, aggregating the first fragment with the second fragment yields the first set of stitching values between the first fragment and the second set of stitching values, and the second set of stitching values between the first set of stitching values and the second fragment. In one particular case, the stitching circuit includes a stitch value modification circuit operable to modify at least one of the second set of stitching values to a transitional value between the last element of the first fragment and the first element of the second fragment. In such a case, aggregating the first fragment with the second fragment includes the modified stitching values between the first fragment and the second fragment. In some cases, the data recovery circuit generates at least one hard decision output corresponding to the combined data set, and wherein the transitional value is generated by the stitch value modification circuit based at least in part on the hard decision output.

In other instances of the aforementioned embodiments, the data recovery circuit includes a data detector circuit, a stitch stripping circuit, and a data decoder circuit. The data detector circuit is operable to apply a data detection algorithm to the combined data set to yield a detected output. The stitch stripping circuit is operable to strip elements of the detected output corresponding to the stitching values from the detected output to yield a decoder input. The data decoder circuit is operable to apply a data decoding algorithm to the decoder input to yield a decoded output.

Other embodiments of the present invention provide data processing systems that include: a stitching circuit and a data recovery circuit. The stitching circuit is operable to: receive a data set including at least a first fragment and a second fragment; calculate at least one stitching value as a transitional value between the last element of the first fragment and the first element of the second fragment; and aggregate the first fragment with the second fragment such that the stitching value is between the first fragment and the second fragment to yield a combined data set. The data recovery circuit is operable to process the combined data set to yield an original data set. In some cases, the system is implemented as part of a communication device. In other instances, the system is implemented as part of a storage device. In particular cases, the system is implemented as part of an integrated circuit.

In some instances of the aforementioned embodiments, the data recovery circuit generates at least one hard decision output corresponding to the combined data set, and the at least one stitching value is calculated based at least in part on the hard decision output. In some cases, the at least one stitching value is calculated based at least in part on the hard decision output, a value of the last element of the first fragment, and a first element of second fragment.

In various instances of the aforementioned embodiments, the data recovery circuit includes: a data detector circuit, a stitch stripping circuit, and a data decoder circuit. The data detector circuit is operable to apply a data detection algorithm to the combined data set to yield a detected output. The detected output includes a hard decision value. The stitch stripping circuit is operable to strip elements of the detected output corresponding to the stitching values from the detected output to yield a decoder input. The data decoder circuit is operable to apply a data decoding algorithm to the decoder input to yield a decoded output. In some cases, the data detection algorithm is a maximum a posteriori data detection algorithm. In other cases, the data detection algorithm is a Viterbi data detection algorithm. In some cases, the data decoding algorithm is a low density parity check algorithm.

Turning to FIG. **1**, a storage system **100** is shown that includes a read channel **110** having enhanced slice stitching circuitry in accordance with one or more embodiments of the present invention. Storage system **100** may be, for example, a hard disk drive. Storage system **100** also includes a preamplifier **170**, an interface controller **120**, a hard disk controller **166**, a motor controller **168**, a spindle motor **172**, a disk platter **178**, and a read/write head **176**. Interface controller **120** controls addressing and timing of data to/from disk platter **178**, and interacts with a host controller (not shown). The data on disk platter **178** consists of groups of magnetic signals that may be detected by read/write head assembly **176** when the assembly is properly positioned over disk platter **178**. In one embodiment, disk platter **178** includes magnetic signals recorded in accordance with either a longitudinal or a perpendicular recording scheme.

In a typical read operation, read/write head **176** is accurately positioned by motor controller **168** over a desired data track on disk platter **178**. Motor controller **168** both positions read/write head **176** in relation to disk platter **178** and drives spindle motor **172** by moving read/write head assembly **176** to the proper data track on disk platter **178** under the direction of hard disk controller **166**. Spindle motor **172** spins disk platter **178** at a determined spin rate (RPMs). Once read/write head **176** is positioned adjacent the proper data track, magnetic signals representing data on disk platter **178** are sensed by read/write head **176** as disk platter **178** is rotated by spindle motor **172**. The sensed magnetic signals are provided as a continuous, minute analog signal representative of the magnetic data on disk platter **178**. This minute analog signal is transferred from read/write head **176** to read channel circuit **110** via preamplifier **170**. Preamplifier **170** is operable to amplify the minute analog signals accessed from disk platter **178**. In turn, read channel circuit **110** decodes and digitizes the received analog signal to recreate the information originally written to disk platter **178**. This data is provided as read data **103** to a receiving circuit. A write operation is substantially the opposite of the preceding read operation with write data **101** being provided to read channel circuit **110**. This data is then encoded and written to disk platter **178**.

In operation, data written to disk platter **178** is split into fragments or portions. When the data is read back from disk platter **178**, the fragments or portions are reassembled and stitched together to yield the original data set. The data processing circuit may be implemented similar to that discussed below in relation to FIG. **4**, FIG. **6** and/or FIG. **8**. The data processing may be completed using a method such as that discussed in either FIG. **9** or FIG. **10** below.

It should be noted that storage system **100** may be integrated into a larger storage system such as, for example, a RAID (redundant array of inexpensive disks or redundant array of independent disks) based storage system. Such a

RAID storage system increases stability and reliability through redundancy, combining multiple disks as a logical unit. Data may be spread across a number of disks included in the RAID storage system according to a variety of algorithms and accessed by an operating system as if it were a single disk. For example, data may be mirrored to multiple disks in the RAID storage system, or may be sliced and distributed across multiple disks in a number of techniques. If a small number of disks in the RAID storage system fail or become unavailable, error correction techniques may be used to recreate the missing data based on the remaining portions of the data from the other disks in the RAID storage system. The disks in the RAID storage system may be, but are not limited to, individual storage systems such as storage system **100**, and may be located in close proximity to each other or distributed more widely for increased security. In a write operation, write data is provided to a controller, which stores the write data across the disks, for example by mirroring or by striping the write data. In a read operation, the controller retrieves the data from the disks. The controller then yields the resulting read data as if the RAID storage system were a single disk.

A data decoder circuit used in relation to read channel circuit **110** may be, but is not limited to, a low density parity check (LDPC) decoder circuit as are known in the art. Such low density parity check technology is applicable to transmission of information over virtually any channel or storage of information on virtually any media. Transmission applications include, but are not limited to, optical fiber, radio frequency channels, wired or wireless local area networks, digital subscriber line technologies, wireless cellular, Ethernet over any medium such as copper or optical fiber, cable channels such as cable television, and Earth-satellite communications. Storage applications include, but are not limited to, hard disk drives, compact disks, digital video disks, magnetic tapes and memory devices such as DRAM, NAND flash, NOR flash, other non-volatile memories and solid state drives.

In addition, it should be noted that storage system **100** may be modified to include solid state memory that is used to store data in addition to the storage offered by disk platter **178**. This solid state memory may be used in parallel to disk platter **178** to provide additional storage. In such a case, the solid state memory receives and provides information directly to read channel circuit **110**. Alternatively, the solid state memory may be used as a cache where it offers faster access time than that offered by disk platted **178**. In such a case, the solid state memory may be disposed between interface controller **120** and read channel circuit **110** where it operates as a pass through to disk platter **178** when requested data is not available in the solid state memory or when the solid state memory does not have sufficient storage to hold a newly written data set. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of storage systems including both disk platter **178** and a solid state memory.

Turning to FIG. **2**, a data transmission system **200** including a receiver **220** enhanced slice stitching circuitry in accordance with one or more embodiments of the present invention. Transmitter **210** transmits encoded data via a transfer medium **230** as is known in the art. The encoded data is received from transfer medium **230** by receiver **220**.

During operation, data sent by transmitter **210** is segregated into fragments or portions. When received by receiver **220**, the fragments or portions are reassembled and stitched together to yield the original data set. The data processing circuit may be implemented similar to that discussed below in relation to FIG. **4**, FIG. **6** and/or FIG. **8**. The data processing may be completed using a method such as that discussed in either FIG. **9** or FIG. **10** below.

Turning to FIG. **3**, another storage system **300** is shown that includes a data processing circuit **310** having enhanced slice stitching circuitry in accordance with one or more embodiments of the present invention. A host controller circuit **305** receives data to be stored (i.e., write data **301**). This data is segregated into fragments or portions by data processing circuit **310** prior to being transferred to a solid state memory access controller circuit **340**. Solid state memory access controller circuit **340** may be any circuit known in the art that is capable of controlling access to and from a solid state memory. Solid state memory access controller circuit **340** formats the received encoded data for transfer to a solid state memory **350**. Solid state memory **350** may be any solid state memory known in the art. In some embodiments of the present invention, solid state memory **350** is a flash memory. Later, when the previously written data is to be accessed from solid state memory **350**, solid state memory access controller circuit **340** requests the data from solid state memory **350** and provides the requested data to data processing circuit **310**. In turn, data processing circuit **310** reassembles and stitches the fragments to yield the original data set. The data processing circuit may be implemented similar to that discussed below in relation to FIG. **4**, FIG. **6** and/or FIG. **8**. The data processing may be completed using a method such as that discussed in either FIG. **9** or FIG. **10** below.

Turning to FIG. **4**, a data transfer circuit **400** is shown that includes a slice reassembly and stitching circuit **445** in accordance with various embodiments of the present invention. Data transfer circuit **400** includes a data encoding circuit **430** that is operable to apply a data encoding algorithm to user write data **405** to yield an encoded output **432**. In some embodiments of the present invention, data encoding circuit **430** applies a low density parity check encoding algorithm as is known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of encoding algorithms and/or combinations of encoding algorithms that may be implemented in accordance with different embodiments of the present invention.

Encoded output **432** is provided to a slicing circuit **440** that segregates encoded output **432** into a number of fragments or portions that are provided as a portion output **442** to a write pre-compensation circuit **450**. FIGS. **5***a*-**5***b* graphically depict a segregated data set **501** that includes segregation of user data **500** into fragments similar to that done by slicing circuit **440**. As shown, a user data **500** in FIG. **5***a* is divided into a data fragment A **510**, a data fragment B **530**, a data fragment C **520**, and a data fragment D **540**. The aforementioned data fragments are divided at boundaries **560**, **570**, **580**. In the case of FIG. **4**, user data **500** corresponds to encoded output **432**, and segregated data set **501** corresponds to portion output **442**. In some cases, the portions of portion output **442** are also interleaved (i.e., shuffled) such that the effects of any localized noise is spread out across different areas. In user data **500**, the data corresponding to Fragment B **530** directly follows the data corresponding to Fragment A **510**; the data corresponding to Fragment C **520** directly follows the data corresponding to Fragment B **530**; and the data corresponding to Fragment D **540** directly follows the data corresponding to Fragment C **520**. The aforementioned interleaving is represented by Fragment C **520** following Fragment A **510**, instead of Fragment B **530** following Fragment A **510**.

Write pre-compensation circuit **450** generates a compensated output **452** that is provided to a data transfer circuit **460**. Data transfer circuit **460** may be any circuit capable of pro-

viding the received information to a transfer medium **470** as a data output **462**. As such, data transfer circuit **460** may be, but is not limited to, a solid state storage device write circuit, a magnetic storage device write circuit, or a data transmission circuit.

Data output **462** is received by an analog front end circuit **415** from medium **470** as a read input **472**. Analog front end circuit **415** processes read input **472** to yield a processed analog signal **417** that is provided to an analog to digital converter circuit **425**. Analog front end circuit **415** may include, but is not limited to, an analog filter and an amplifier circuit as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of circuitry that may be included as part of analog front end circuit **415**. Analog to digital converter circuit **425** converts processed analog signal **417** into a corresponding series of digital samples **427**. Analog to digital converter circuit **425** may be any circuit known in the art that is capable of producing digital samples corresponding to an analog input signal. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of analog to digital converter circuits that may be used in relation to different embodiments of the present invention. Digital samples **427** are provided to an equalizer circuit **435**. Equalizer circuit **435** applies an equalization algorithm to digital samples **427** to yield an equalized output **437**. In some embodiments of the present invention, equalizer circuit **435** is a digital finite impulse response filter circuit as are known in the art.

Equalized output **437** is provided to slice reassembly and stitching circuit **445**. Slice reassembly and stitching circuit **445** is operable to replicate some of the instances of equalized output **437** at the boundaries of the respective samples. In one particular embodiment of the present invention, three instances of equalized output **437** on either side of a given fragment are replicated. Turning to FIG. **5***c*, the instance replication is shown. In particular, at the end of data fragment A **510**, the last three instances data fragment A **510** in equalized output **437** are replicated as stitching bits **514**. At the beginning of data fragment C **520**, the first three instances data fragment C **520** in equalized output **437** are replicated as stitching bits **522**. At the end of data fragment C **520**, the last three instances data fragment C **520** in equalized output **437** are replicated as stitching bits **524**. At the beginning of data fragment B **530**, the first three instances data fragment B **530** in equalized output **437** are replicated as stitching bits **532**. At the end of data fragment B **530**, the last three instances data fragment B **530** in equalized output **437** are replicated as stitching bits **534**. At the beginning of data fragment D **540**, the first three instances data fragment D **540** in equalized output **437** are replicated as stitching bits **542**.

Slice reassembly and stitching circuit **445** assembles the respective fragments along with the replicated instances of equalized output **437** to yield an overall data set. Turning to FIG. **5***d*, an example of the resulting overall data set **503** is shown. As shown, data fragment A **510** plus stitching bits **514** precede data fragment C **530** plus stitching bits **522** and stitching bits **524**. Data fragment C **520** plus stitching bits **522** and stitching bits **524** precedes data fragment B **530** plus stitching bits **532** and stitching bits **534**. Data fragment B **530** plus stitching bits **532** and stitching bits **534** precedes data fragment D **540** plus stitching bits **542**.

Slice reassembly and stitching circuit **445** then stitches the boundaries between the stitching bits. In one particular embodiment of the present invention, the stitching simply includes appending stitching bits **522** to stitching bits **514**, appending stitching bits **532** to stitching bits **524**, and appending stitching bits **542** to stitching bits **534**. FIG. **6** shows a detailed block diagram of a data reassembly and stitching circuit **600** that may be used in place of slice reassembly and stitching circuit **445** in accordance with one or more embodiments of the present invention. Data reassembly and stitching circuit **600** includes a fragment counter circuit **610** that is incremented as each instance of equalized output **437** is received. The resulting count value **612** indicates the beginning and end of fragments in equalized output **437**. Once the end of a fragment is indicated by count value **612**, fragment counter circuit **610** is reset to indicate the beginning of the next fragment.

Count value **612** is provided to an oversampled fragment buffer circuit **620** that stores instances of equalized output **437**, and replicates instances of equalized output at the beginning and end of each fragment. The respective fragments are provided as a fragment output **622**, a preceding stitching bits (e.g., stitching bits **522**, stitching bits **532**, and stitching bits **542**) are provided as preceding stitching bits **624**, and stitching bits (e.g., stitching bits **514**, stitching bits **524**, and stitching bits **534**) are provided as succeeding stitching bits **626**. Fragment output **622**, preceding stitching bits **624**, and succeeding stitching bits **626** are provided to an oversampled fragment recombination circuit **660** that assembles the various portions to make oversampled packets (e.g., Fragment C **520** plus stitching bits **522** and stitching bits **524**; Fragment B **530** plus stitching bits **532** and stitching bits **534**). These oversampled packets are then provided to data detecting circuit **455** as a detector input **447**.

Data detecting circuit **455** may be any circuit known in the art that is capable of apply a data detection algorithm to a data set to yield a detected output. As some examples, data detecting circuit **455** may be, but is not limited to, a Viterbi algorithm detector circuit or a maximum a posteriori detector circuit as are known in the art. Of note, the general phrases "Viterbi data detection algorithm" or "Viterbi algorithm data detector circuit" are used in their broadest sense to mean any Viterbi detection algorithm or Viterbi algorithm detector circuit or variations thereof including, but not limited to, bi-direction Viterbi detection algorithm or bi-direction Viterbi algorithm detector circuit. Also, the general phrases "maximum a posteriori data detection algorithm" or "maximum a posteriori data detector circuit" are used in their broadest sense to mean any maximum a posteriori detection algorithm or detector circuit or variations thereof including, but not limited to, simplified maximum a posteriori data detection algorithm and a max-log maximum a posteriori data detection algorithm, or corresponding detector circuits. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data detecting circuits that may be used in relation to different embodiments of the present invention. Detected output **457** may include both hard decisions and soft decisions. The terms "hard decisions" and "soft decisions" are used in their broadest sense. In particular, "hard decisions" are outputs indicating an expected original input value (e.g., a binary '1' or '0', or a non-binary digital value), and the "soft decisions" indicate a likelihood that corresponding hard decisions are correct. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of hard decisions and soft decisions that may be used in relation to different embodiments of the present invention. The hard decisions from detected output **457** are provided as a hard decision output **456** from data detecting circuit **455** to slice reassembly and stitching circuit **445**.

Turning to FIG. **7***a*, data stitching without stitch value modification such as that discussed in relation to FIG. **6** is graphically depicted in accordance with some embodiments of the present invention. Equalized output **437** is shown jux-

taposed with hard decision output **456**. As shown, there is a severe transition **710** (i.e., from +22 to −22) where stitching bits **532** are appended to stitching bits **524**. Such a severe transition may disrupt operation of data detecting circuit **455** that may rely on a reasonably continuous signal input.

In other embodiments of the present invention, the severity of the transition is mitigated by stitching processes that modify one or more of the stitching bits between succeeding data fragments. Such stitching processes include: modifying one or more of stitching bits **514** and stitching bits **522** to smooth a transition between the last instance of data fragment A **510** and the first instance of data fragment C **520**; modifying one or more of stitching bits **524** and stitching bits **532** to smooth a transition between the last instance of data fragment C **520** and the first instance of data fragment B **530**; and modifying one or more of stitching bits **534** and stitching bits **542** to smooth a transition between the last instance of data fragment B **530** and the first instance of data fragment D **540**. Smoothing the transition between succeeding data fragments avoids disrupting operation of a data detecting circuit **455** caused by severe discontinuities between fragments.

FIG. **8** shows a detailed block diagram of a data reassembly and stitching circuit **800** that may be used in place of slice reassembly and stitching circuit **445** in accordance with one or more embodiments of the present invention using a stitch modification process. Data reassembly and stitching circuit **800** includes a fragment counter circuit **810** that is incremented as each instance of equalized output **437** is received. The resulting count value **812** indicates the beginning and end of fragments in equalized output **437**. Once the end of a fragment is indicated by count value **812**, fragment counter circuit **810** is reset to indicate the beginning of the next fragment.

Count value **812** is provided to an oversampled fragment buffer circuit **820** that stores instances of equalized output **437**, and replicates instances of equalized output at the beginning and end of each fragment. The respective fragments are provided as a fragment output **822**, a preceding stitching bits (e.g., stitching bits **522**, stitching bits **532**, and stitching bits **542**) are provided as preceding stitching bits **824**, and stitching bits (e.g., stitching bits **514**, stitching bits **524**, and stitching bits **534**) are provided as succeeding stitching bits **826**. Preceding stitching bits **824**, succeeding stitching bits **826**, and hard decision output **456** are provided to a stitch value modification circuit **850**.

Stitch value modification circuit **850** modifies one or more stitch values based upon hard decision output **456**. Each sample (including the stitch values) received as equalized output **437** can be expressed as:

$$\text{Equalized Output}_k = \text{Ideal Equalized Output}_k + n_k,$$

where k indicates the particular instance of equalized output **437**, and n_k is the noise included in each instance of equalized output **437**. The preceding may be expressed as:

$$\text{Equalized Output}_k = \sum_{j=0}^{L-1} (\text{Hard Decision Output}_{k-j} T_j) + n_k,$$

where T_k is the target value used in a target filter to yield the ideal equalized output, and L is the target length. In some embodiments of the present invention, stitch value modification circuit **850** modifies three stitch values immediately preceding a fragment while leaving other stitch values unmodified. Using FIG. **7***b* as an example, stitching bits **524** are not modified and stitching bits **532** are modified to yield stitching bits **720**. In FIG. **7***b*, equalized output **437** is shown juxtaposed with hard decision output **456**. As shown, there is a smoothed transition **730** by modifying the values of stitching bits **532** to yield modified stitching bits **720** where stitching bits **532** are appended to stitching bits **524**. Such a smoothed transition is less likely to disrupt operation of data detecting circuit **455** when compared with a more severe transition. The value of modified stitching values **720** may be expressed as:

$$\text{Modified Stitching Values}_k = \sum_{j=0}^{L-1} (\text{Modified Hard Decision Output}_{k-j} T_j) + \text{Equalized Output}_k - \sum_{j=0}^{L-1} (\text{Hard Decision Output}_{k-j} T_j),$$

where the modified hard decision output is the hard decision corresponding to the modified stitching values. As shown in FIG. **7***b*, by applying the stitch value modification as previously discussed, modified stitching values **720** are changed from −22, −22, −22 to 10, −12, −20, respectively.

The resulting modified stitch values **852** generated by stitch value modification circuit **850** are provided along with fragment output **822** to an oversampled fragment recombination circuit **860** that assembles the various portions to make oversampled packets (e.g., Fragment C **520** plus stitching bits **522** and stitching bits **524**; Fragment B **530** plus stitching bits **532** and stitching bits **534**). These oversampled packets are then provided to data detecting circuit **455** as detector input **447**.

Detected output **457** is provided to a stitch stripping circuit **463**. Stitch stripping circuit **463** de-interleaves the data sets (i.e., puts the fragments in the original order provided by data encoding circuit **430**) and removes the stitching bits from between the fragments (either stitching bits or modified stitching bits) to yield a decoder input **464**. Turning to FIG. **5***e*, an example of a de-interleaved and stitch removed data set **504**. As shown, de-interleaved and stitch removed data set **504** includes data fragment A **510** followed by data fragment B **530**, data fragment B **530** is followed by data fragment C **520**, and data fragment C **520** is followed by data fragment D **540**.

Decoder input **464** is provided to a data decoding circuit **465** that applies a data decoding algorithm to the received input to yield a decoded output **467**. In one particular embodiment of the present invention, data decoding circuit **465** is operable to apply a low density parity check decoded circuit. Where decoded output **467** fails to converge (i.e., fails to reflect the original data), it is provided as a feedback **468** to data detecting circuit **455** to apply another iteration of the combination of data detecting circuit **455** and data decoding circuit **465**. Alternatively, where decoded output **467** does converge (i.e., reflects the original data), it is provided to a hard decision output circuit **475** that provides the resulting hard decisions as user read data **477**.

Turning to FIG. **9**, a flow diagram **900** shows a method in accordance with some embodiments of the present invention for data reassembly and stitching without stitch value modification. Following flow diagram **900**, an equalized output is received (block **902**). The equalized output may be derived, for example, from data accessed from a storage medium or a transmission medium. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of sources from which the equalized output may be derived. An element counter is incremented as each instance of the

equalized output is received (block **904**). This element counter is responsible for indicating the beginning and end of fragments within the equalized outputs. Once the end of a fragment is indicated, the counter is reset indicating the beginning of the subsequent fragment. In addition, each element of the equalized output is stored to a fragment buffer (block **906**).

Based upon the element counter it is determined whether the start of a fragment has been found (block **910**). Where the start of a fragment has been found (block **910**), a fragment start pointer is set to point N elements before the start of the fragment in the fragment buffer (block **915**). The N elements preceding the fragment are the preceding stitching bits (i.e., preceding stitch) that are set equal to the value of the first element of the fragment. Alternatively, where the start of a fragment has not been found (block **910**), it is determined whether an end of fragment has occurred (block **920**). Where the end of a fragment has been found (block **920**), a fragment end pointer is set to point M elements beyond the end of the fragment (block **930**). The M elements succeeding the fragment are the current succeeding stitching bits (i.e., succeeding stitch) that are set equal to the value of the last element of the fragment.

The user data portion of the fragment (i.e., everything but the preceding stitch and the succeeding stitch) is pulled from the fragment buffer (block **935**). In addition, the succeeding stitch and the preceding stitch are also pulled from the fragment buffer (block **940**). The preceding stitch, the succeeding switch, and the user data portion are assembled into a complete data set (block **945**). An example of such a complete data set is shown in FIG. **5***d* including data fragment C**530** preceded by stitching bits **522** and stitching bits **524**.

It is then determined if sufficient complete data sets have been received to form a complete sector of data (block **950**). A sector is the size of an original encoded data set prior to being segregated into fragments. In some embodiments of the present invention, a sector is 4K bits. Where sufficient complete data sets have been received (block **950**), the complete data sets are appended one to another and a data detection algorithm is applied to the complete data set to yield a detected output (block **955**). The appended complete data sets may be similar to that shown as overall data set **503** of FIG. **5***d*. The data detection algorithm may be any data detection algorithm known in the art including, but not limited to, a Viterbi data detection algorithm or a maximum a posteriori data detection algorithm. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data detection algorithms that may be used in relation to different embodiments of the present invention. The stitch bits are then stripped from the appended complete data sets and where applicable the data sets are un-shuffled to yield a decoder input (block **960**). The decoder input may look similar to de-interleaved and stitch removed data set **504** of FIG. **5***e*. A data decoding algorithm is then applied to the decoder input to yield a decoded output (block **965**). The data decoding algorithm may be, for example, a low density parity check decoding algorithm as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data decoding algorithms that may be used in relation to different embodiments of the present invention.

Turning to FIG. **10**, a flow diagram **1000** shows a method in accordance with other embodiments of the present invention for data reassembly and stitching including stitch value modification. Following flow diagram **1000**, an equalized output is received (block **1002**). The equalized output may be derived, for example, from data accessed from a storage medium or a transmission medium. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of sources from which the equalized output may be derived. An element counter is incremented as each instance of the equalized output is received (block **1004**). This element counter is responsible for indicating the beginning and end of fragments within the equalized outputs. Once the end of a fragment is indicated, the counter is reset indicating the beginning of the subsequent fragment. In addition, each element of the equalized output is stored to a fragment buffer (block **1006**).

Based upon the element counter it is determined whether the start of a fragment has been found (block **1010**). Where the start of a fragment has been found (block **1010**), a fragment start pointer is set to point N elements before the start of the fragment in the fragment buffer (block **1015**). The N elements preceding the fragment are the preceding stitching bits (i.e., preceding stitch) that are set equal to the value of the first element of the fragment. Alternatively, where the start of a fragment has not been found (block **1010**), it is determined whether an end of fragment has occurred (block **1020**). Where the end of a fragment has been found (block **1020**), the current succeeding stitch is stored as the preceding succeeding stitch (block **1025**). In addition, a fragment end pointer is set to point M elements beyond the end of the fragment (block **1030**). The M elements succeeding the fragment are the current succeeding stitching bits (i.e., succeeding stitch) that are set equal to the value of the last element of the fragment.

The user data portion of the fragment (i.e., everything but the preceding stitch and the succeeding stitch) is pulled from the fragment buffer (block **1035**). In addition, the succeeding stitch and the preceding stitch are also pulled from the fragment buffer (block **1040**). An updated preceding stitch is calculated based upon current hard decision data and the preceding succeeding switch (block **1045**). Referring to FIGS. **4**, **5***d* and **7***b*, the stitch value modification results in modifying one or more stitch values based upon hard decision outputs resulting from application of a data detection algorithm. Each sample (including the stitch values) received as the equalized output (block **1002**) can be expressed as:

$$\text{Equalized Output}_k = \text{Ideal Equalized Output}_k + n_k,$$

where k indicates the particular instance of the equalized output, and n_k is the noise included in each instance of the equalized output. The preceding may be expressed as:

$$\text{Equalized Output}_k = \sum_{j=0}^{L-1} (\text{Hard Decision Output}_{k-j} T_j) + n_k,$$

where T_k is the target value used in a target filter to yield the ideal equalized output, and L is the target length. In some embodiments of the present invention, the stitch value modification modifies three stitch values immediately preceding a fragment while leaving other stitch values unmodified. Using FIG. **7***b* as an example, stitching bits **524** are not modified and stitching bits **532** are modified to yield stitching bits **720**. In FIG. **7***b*, equalized output **437** is shown juxtaposed with hard decision output **456**. As shown, there is a smoothed transition **730** by modifying the values of stitching bits **532** to yield modified stitching bits **720** where stitching bits **532** are appended to stitching bits **524**. Such a smoothed transition is less likely to disrupt operation of data detecting circuit **455** when compared with a more severe transition. The value of modified stitching values **720** may be expressed as:

$$\text{Modified Stitching Values}_k = \sum_{j=0}^{L-1} (\text{Modified Hard Decision Output}_{k-j} T_j) +$$

$$\text{Equalized Output}_k - \sum_{j=0}^{L-1} (\text{Hard Decision Output}_{k-j} T_j),$$

where the modified hard decision output is the hard decision corresponding to the modified stitching values. As shown in FIG. **7***b*, by applying the stitch value modification as previously discussed, modified stitching values **720** are changed from −22, −22, −22 to 10, −12, −20, respectively.

The updated preceding stitch, the fragment, and the current succeeding stitch are assembled into a complete data set (block **1050**). A data detection algorithm is applied to the complete data set to yield a detected output (block **1055**). The detected output includes updated current hard decision data. The data detection algorithm may be any data detection algorithm known in the art including, but not limited to, a Viterbi data detection algorithm or a maximum a posteriori data detection algorithm. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data detection algorithms that may be used in relation to different embodiments of the present invention. It is then determined if sufficient detected outputs have been received to form a complete sector of data (block **1060**). A sector is the size of an original encoded data set prior to being segregated into fragments. In some embodiments of the present invention, a sector is 4K bits. Where sufficient complete data sets have been received (block **1060**), the stitch bits are stripped from the detected output and the various fragments are reordered (i.e., de-interleaved) where applicable to yield a decoder input (block **1065**). The decoder input may look similar to de-interleaved and stitch removed data set **504** of FIG. **5***e*. A data decoding algorithm is then applied to the decoder input to yield a decoded output (block **1070**). The data decoding algorithm may be, for example, a low density parity check decoding algorithm as are known in the art. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of data decoding algorithms that may be used in relation to different embodiments of the present invention.

It should be noted that the various blocks discussed in the above application may be implemented in integrated circuits along with other functionality. Such integrated circuits may include all of the functions of a given block, system or circuit, or a subset of the block, system or circuit. Further, elements of the blocks, systems or circuits may be implemented across multiple integrated circuits. Such integrated circuits may be any type of integrated circuit known in the art including, but are not limited to, a monolithic integrated circuit, a flip chip integrated circuit, a multichip module integrated circuit, and/or a mixed signal integrated circuit. It should also be noted that various functions of the blocks, systems or circuits discussed herein may be implemented in either software or firmware. In some such cases, the entire system, block or circuit may be implemented using its software or firmware equivalent. In other cases, the one part of a given system, block or circuit may be implemented in software or firmware, while other parts are implemented in hardware.

In conclusion, the invention provides novel systems, devices, methods and arrangements for data processing. While detailed descriptions of one or more embodiments of the invention have been given above, various alternatives, modifications, and equivalents will be apparent to those skilled in the art without varying from the spirit of the invention. Therefore, the above description should not be taken as limiting the scope of the invention, which is defined by the appended claims.

What is claimed is:

1. A data processing system, the system comprising:

a stitching circuit operable to:

receive a data set including at least a first fragment and a second fragment;

replicate data from at least one of the first fragment and the second fragment as stitching values;

aggregate the first fragment with the second fragment with the stitching values between the first fragment and the second fragment to yield a combined data set; and

a data recovery circuit operable to process the combined data set to yield an original data set.

2. The system of claim **1**, wherein the stitching circuit comprises:

a stitch value modification circuit operable to modify at least one of the stitching values to a transitional value between a last element of the first fragment and a first element of the second fragment to yield a modified stitching value; and

wherein aggregating the first fragment with the second fragment includes the modified stitching value between the first fragment and the second fragment.

3. The system of claim **2**, wherein the data recovery circuit generates at least one hard decision output corresponding to the combined data set, and wherein the transitional value is generated by the stitch value modification circuit based at least in part on the hard decision output.

4. The system of claim **2**, wherein the transitional value smoothes a discontinuity between the first fragment and the second fragment.

5. The system of claim **1**, replicating data from at least one of the first fragment and the second fragment as stitching values comprises:

replicating a first value from the first fragment as a first set of stitching values;

replicating a second value from the second fragment as a second set of stitching values; and

wherein aggregating the first fragment with the second fragment yields the first set of stitching values between the first fragment and the second set of stitching values, and the second set of stitching values between the first set of stitching values and the second fragment.

6. The system of claim **5**, wherein the stitching circuit comprises:

a stitch value modification circuit operable to modify at least one of the second set of stitching values to a transitional value between a last element of the first fragment and a first element of the second fragment to yield a modified stitching value; and

wherein aggregating the first fragment with the second fragment includes the modified stitching values between the first fragment and the second fragment.

7. The system of claim **6**, wherein the data recovery circuit generates at least one hard decision output corresponding to the combined data set, and wherein the transitional value is generated by the stitch value modification circuit based at least in part on the hard decision output.

8. The system of claim **1**, wherein the data recovery circuit comprises:

a data detector circuit operable to apply a data detection algorithm to the combined data set to yield a detected output;

a stitch stripping circuit operable to strip elements of the detected output corresponding to the stitching values from the detected output to yield a decoder input; and

a data decoder circuit operable to apply a data decoding algorithm to the decoder input to yield a decoded output.

9. The system of claim **1**, wherein the system is implemented as part of a device selected from a group consisting of: a communication device, and a storage device.

10. The system of claim **1**, wherein the system is implemented as part of an integrated circuit.

11. A data processing system, the system comprising:

a stitching circuit operable to:

receive a data set including at least a first fragment and a second fragment;

calculate at least one stitching value as a transitional value between a last element of the first fragment and a first element of the second fragment;

aggregate the first fragment with the second fragment such that the stitching value is between the first fragment and the second fragment to yield a combined data set; and

a data recovery circuit operable to process the combined data set to yield an original data set.

12. The system of claim **11**, wherein the data recovery circuit generates at least one hard decision output corresponding to the combined data set, and wherein the at least one stitching value is calculated based at least in part on the hard decision output.

13. The system of claim **12**, wherein the at least one stitching value is calculated based at least in part on the hard decision output, a value of the last element of the first fragment, and a first element of second fragment.

14. The system of claim **11**, wherein the data recovery circuit comprises:

a data detector circuit operable to apply a data detection algorithm to the combined data set to yield a detected output, wherein the detected output includes a hard decision value;

a stitch stripping circuit operable to strip elements of the detected output corresponding to the at least one stitching values from the detected output to yield a decoder input; and

a data decoder circuit operable to apply a data decoding algorithm to the decoder input to yield a decoded output.

15. The system of claim **14**, wherein the data detection algorithm is selected from a group consisting of: a maximum a posteriori data detection algorithm, and a Viterbi data detection algorithm.

16. The system of claim **14**, wherein the data decoding algorithm is a low density parity check algorithm.

17. The system of claim **14**, wherein the at least one stitching value is calculated based at least in part on the hard decision output.

18. The system of claim **11**, wherein the system is implemented as part of a device selected from a group consisting of: a communication device, and a storage device.

19. The system of claim **11**, wherein the system is implemented as part of an integrated circuit.

20. A hard disk drive, the hard disk drive comprising:

a disk platter including a stored information;

a head assembly disposed in relation to the disk platter and operable to:

sense the stored information to yield sensed information;

provide a signal corresponding to the sensed information;

an analog to digital converter circuit operable to convert the sensed information to a series of digital samples;

an equalizer circuit operable to equalize the digital samples to yield an equalized output, wherein the equalized output includes a first fragment of data and a second fragment of data;

a stitching circuit operable to:

calculate at least one stitching value as a transitional value between a last element of the first fragment of data and a first element of the second fragment of data;

aggregate the first fragment of data with the second fragment of data such that the at least one stitching value is between the first fragment of data and the second fragment of data to yield a combined data set; and

a data detector circuit operable to apply a data detection algorithm to the combined data set to yield a detected output, wherein the detected output includes a hard decision value;

a stitch stripping circuit operable to strip elements of the detected output corresponding to the at least one stitching values from the detected output to yield a decoder input;

a data decoder circuit operable to apply a data decoding algorithm to the decoder input to yield a decoded output; and

wherein the at least one stitching value is calculated based at least in part on the hard decision output, a value of the last element of the first fragment, and a first element of second fragment.

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